

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

15/D.

In re the Application of:

Bailey et al.

Docket No.: TI-27935

Serial No.: 09/452,691

Examiner: Fenty, J.

Filed: 12/02/99

Art Unit: 2815

For: AN INTEGRATED CIRCUIT HAVING A THIN FILM RESISTOR
LOCATED WITHIN A MULTILEVEL DIELECTRIC BETWEEN AN
UPPER AND LOWER METAL INTERCONNECT LAYERAmendment under 37 CFR 1.111

FAX RECEIVED

Assistant Commissioner of Patents
Washington, DC 20231

APR 04 2003

TECHNOLOGY CENTER 2800

Dear Sir:

The following amendments and remarks are offered in response to the Examiner's Office Action dated 10/03/2002. They are respectfully submitted as a full and complete response to that Action.

Please amend the above-referenced application as follows:

In the Claims:

Amend claim 1 to read as follows:

1. (twice amended) An integrated circuit comprising:
a lower metal interconnect layer located over a semiconductor body;
a multi-level dielectric layer located over said lower interconnect layer;
an upper metal interconnect layer located over said multi-level dielectric
layer; and
a thin film resistor embedded within said multi-level dielectric layer
between said lower metal interconnect layer and said upper metal interconnect